What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a first region formed with a circuit element and provided with a plurality of circuit element connecting pads to which said circuit element is connected, and a second region surrounding the periphery of said first region;

a first external terminal having a plurality of first sub-external terminals disposed on said first region and composed of terminals to be grounded and terminals to be connected to a power source, and a plurality of second sub-external terminals disposed on said first region;

a plurality of second external terminals disposed on said second region;

a first wiring structure having a first sub-wiring structure provided on said first region for electrically connecting said plurality of first sub-external terminals and said plurality of circuit element connecting pads, and a second sub-wiring structure provided on said first region for electrically connecting said plurality of second sub-external terminals and said plurality of circuit element connecting pads; and

a plurality of second wiring structures provided from said first region to said second region for electrically connecting said plurality of second external terminals and said plurality of circuit element connecting pads.

2. The semiconductor device according to claim 1,

wherein the surface area of a cross section of said first sub-wiring structure severed in an orthogonal direction to the direction of extension thereof is set to be greater than the surface area of a cross section of each of said first wiring structure and second wiring structure severed in an orthogonal direction to the direction of extension thereof.

3. The semiconductor device according to claim 1, wherein each of the first wiring structures, having said plurality of first sub-wiring structures and second sub-wiring structures, includes a first rewiring layer which is electrically connected to one of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer to one of said first external terminals having said plurality of first sub-external terminals and second sub-external terminals, and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, and a second post portion for electrically connecting said second rewiring layer to one of said plurality of second external terminals.

4. The semiconductor device according to claim 2, wherein each of the first wiring structures, having said plurality of first sub-wiring structures and second sub-wiring structures, includes a first rewiring layer which is electrically connected to one of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer

to one of said first external terminals comprising said plurality of first sub-external terminals and second sub-external terminals, and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, and a second post portion for electrically connecting said second rewiring layer to one of said plurality of second external terminals.

5. A semiconductor device comprising:

a semiconductor substrate having a first region formed with a circuit element and provided with a plurality of circuit element connecting pads to which said circuit element is connected, and a second region surrounding the periphery of said first region;

a metallic layer provided on said second region;

an insulating film provided such that a part of said circuit element connecting pads and a part of said metallic layer are exposed;

a plurality of first wiring structures provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads;

a plurality of second wiring structures provided on said insulating film from said first region to said second region and electrically connected to said plurality of circuit element connecting pads;

a plurality of third wiring structures provided on

said insulating film in said second region and electrically connected to said exposed metallic layer;

a sealing portion provided such that a part of said first wiring structures is exposed and such that a part of said second wiring structures and third wiring structures is exposed in said second region;

a plurality of first external terminals disposed on said first region and connected to said first wiring structures; and

a plurality of second external terminals disposed on said second region and connected to one or both of said second wiring structures and said third wiring structures.

6. The semiconductor device according to claim 5, wherein the surface area of a cross section of said third wiring structure severed in an orthogonal direction to the direction of extension thereof is set to be greater than the surface area of a cross section of each of said first wiring structure and second wiring structure severed in an orthogonal direction to the direction of extension thereof.

7. The semiconductor device according to claim 5, wherein said metallic layer is formed from an identical material to any one of the first sub-wiring structure, second sub-wiring structure, first wiring structure, second wiring structure, and third wiring structure.

8. The semiconductor device according to claim 5, wherein each of said plurality of first wiring structures includes a first rewiring layer which is electrically connected to one

of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer to one of said plurality of first external terminals, and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, a third rewiring layer connected to said third wiring structure formed on said second region, and a second post portion for electrically connecting one or both of said second rewiring layer and said third rewiring layer to one of said plurality of second external terminals.

9. The semiconductor device according to claim 6, wherein each of said plurality of first wiring structures includes a first rewiring layer which is electrically connected to one of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer to one of said plurality of first external terminals, and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, a third rewiring layer connected to said third wiring structure formed on said second region, and a second post portion for electrically connecting one or both of said second rewiring layer and said third rewiring layer to one of said plurality of second external terminals.

10. A semiconductor device comprising:

a semiconductor substrate having a first region

formed with a circuit element and provided with a plurality of circuit element connecting pads to which said circuit element is connected, and a second region surrounding the periphery of said first region;

a metallic layer provided on said second region;

an insulating film provided such that a part of said circuit element connecting pads and a part of said metallic layer are exposed;

a first wiring structure having a first sub-wiring structure provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads, and a second sub-wiring structure provided on said insulating film in said first region and electrically connected to said plurality of circuit element connecting pads;

a plurality of second wiring structures provided on said insulating film from said first region to said second region and electrically connected to said circuit element connecting pads;

a plurality of third wiring structures provided on said insulating film in said second region and electrically connected to said exposed metallic layer;

a sealing portion provided such that a part of said first sub-wiring structure and said second sub-wiring structure is exposed, and such that a part of said second wiring structure and said third wiring structure in said second region is exposed;

a first external terminal having a plurality of first sub-external terminals disposed on said first region and composed

of terminals to be connected to a power source, and a plurality of second sub-external terminals disposed on said first region; and

a plurality of second external terminals disposed on said second region and connected to one or both of said second wiring structure and said third wiring structure.

11. The semiconductor device according to claim 10, wherein the surface area of a cross section of said third wiring structure and said first sub-wiring structure severed in an orthogonal direction to the direction of extension thereof is set to be greater than the surface area of a cross section of each of said first wiring structure and second wiring structure severed in an orthogonal direction to the direction of extension thereof.

12. The semiconductor device according to claim 10, wherein said metallic layer is formed from an identical material to any one of the first sub-wiring structure, second sub-wiring structure, first wiring structure, second wiring structure, and third wiring structure.

13. The semiconductor device according to claim 10, wherein each of the first wiring structures, having said plurality of first sub-wiring structures and second sub-wiring structures, comprises a first rewiring layer which is electrically connected to one of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer to one of said first external terminals comprising said plurality of first sub-external terminals and second sub-external terminals,

and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, a third rewiring layer connected to said third wiring structure formed on said second region, and a second post portion for electrically connecting one or both of said second rewiring layer and said third rewiring layer to one of said plurality of second external terminals.

14. The semiconductor device according to claim 11, wherein each of the first wiring structures, having said plurality of first sub-wiring structures and second sub-wiring structures, includes a first rewiring layer which is electrically connected to one of said circuit element connecting pads, and a first post portion for electrically connecting said first rewiring layer to one of said first external terminals comprising said plurality of first sub-external terminals and second sub-external terminals, and

each of said plurality of second wiring structures includes a second rewiring layer provided from said first region to said second region and electrically connected to one of said circuit element connecting pads, a third rewiring layer connected to said third wiring structure formed on said second region, and a second post portion for electrically connecting one or both of said second rewiring layer and said third rewiring layer to one of said plurality of second external terminals.